Issue: 01 / Volume 01 / Jan 2020

BUILDERS ENGINEERING COLLEGE

A NEWSLETTER OF

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT - VISION & MISSION

VISION

To be an updated technocrat in the field of Electronics and Communication Engineering.

MISSION

Preparing rural students for successful career through creative thinking and knowledge application

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Vision of the Institution

To be the most preferred knowledge provider.

Mission of the Institution

Builders Engineering College endeavors to prepare rural students for successful career through academic and applied research.

About the Department

Established in 2009, the Department commenced with an initial intake of 60 students. It boasts 10 fully-equipped laboratories, each adhering to university norms and furnished with cutting-edge technology.

The ECE Computer Centre provides students access to special software packages such as MENTOR GRAPHICS, PSPICE, MATLAB, Xilinx ISE, MULTISIM, MODELSIM, and KIEL.

The department stands out with its distinctive offerings, including advanced trainer kits, ARM Processors, Altera development boards, CPLD Trainer kits, and Wireless Sensor Networks trainer kits. These resources empower students to engage in real-time projects and practical learning experiences.

The department actively engages with professional bodies such as IEEE, IETE, and ISTE, providing a valuable platform for both faculty members and students.

Programme Specific Outcomes (PSOs)

- To design and develop complex systems in the research areas of next generation Communication Systems, RF and Power systems.
- To design and develop systems in the domains of IoT based Embedded Systems, Advanced Signal and Image Processing and latest Semiconductor technologies.

Program Educational Objectives (PEOs)

- Shall be successful in their professional careers, academic pursuits and research
- Shall study and build abilities on a continual basis in order to deliver high-impact, energy-efficient and futuristic solutions
- Shall demonstrate strong communication skills, a professional mindset and ethics in order to create and build real-world multidisciplinary solutions that are technically sound, economically feasible, and socially acceptable.

Principal's Message

It is a matter of great pride and satisfaction for Builders Engineering College to bring out the News Letter, Released from the Department of ECE. The College has made tremendous progress in all areas academic, non-academic, capacity building relevant to staff and students. I am confident that this issue of the Department News Letter will send a positive signal to the staff, students, and the person who are interested in Technical education and Technology-based activities.

I congratulate the Editorial Board of this News Letter who have played a wonderful role in accomplishing the task in Record time.

I express my deep sense of gratitude to Dr. S. Kumar, HoD/ECE under whose guidance this Technical work has been undertaken and completed within the stipulated time.

Also my heartfelt Congratulations to staff members and Students for their fruitful effort.

Dr. S. Gopalakrishnan
Principal

Words from Head of the Department

Dear Members of ECE community,

I am delighted to express my congratulations on the unveiling of the Electronics and Communication Engineering (ECE) Newsletter. This publication stands as a testament to the remarkable progress achieved in diverse realms, covering both academic and non-academic spheres. It also highlights the ongoing development of capabilities relevant to our esteemed staff and students. I commend the Editorial Board for their praiseworthy role in accomplishing this task with remarkable efficiency and within a record timeframe. I extend my sincere gratitude to Mr. U. Rajasekaran, AP/ECE for providing invaluable guidance.

My warmest congratulations to the dedicated staff members and enthusiastic students who have invested their time and effort into bringing this newsletter to life. Your collective contributions have undeniably played a pivotal role in the success of this publication.

Dr. S. Kumar
Head of the Department

Editor's Desk

Dear Readers,

Welcome to the latest edition of our Electronics and Communication Department Newsletter! As we navigate the dynamic and ever-evolving world of technology, we are thrilled to share with you the latest developments, achievements, and exciting projects from our department.

We are proud to highlight the accomplishments of our students and faculty, who continue to push the boundaries of knowledge and contribute to advancements in the field.

Our commitment to fostering a collaborative and forward-thinking community is evident in the various events and activities featured in this newsletter. From guest lectures by industry experts to workshops and hackathons, we strive to provide our students with opportunities to engage with real-world challenges and enhance their skills.

As we embark on another semester filled with promise and potential, we extend our gratitude to our dedicated faculty, enthusiastic students, and supportive community. Together, we are shaping the future of electronics and communication, and we are excited to have you join us on this journey.

Thank you for your continued interest and support. We hope you enjoy reading this edition of our newsletter and stay tuned for more updates from the Electronics and Communication Department.

Best regards,

Mr. U. Rajasekaran, AP/ECE
Managing Editor

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EVENTS ORGANIZED

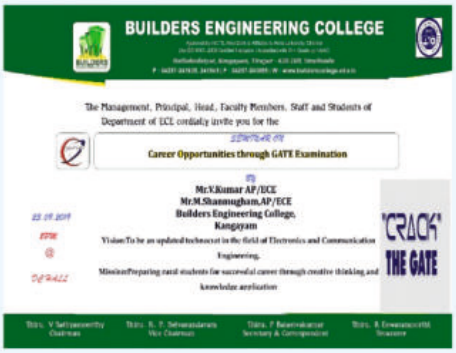
"Job Opportunities in VLSI Design"

October 4, 2019

On October 4, 2019, a session on "Job Opportunities in VLSI Design" was organized by the student association "GNAANA" and the Indian Society for Technical Education (ISTE) at Builders Engineering College, Kangayam. The session was conducted by Mr. U. Rajasekaran, and Mr. M. Prakash,.The focus of the session was to enlighten students about career prospects and opportunities in the field of Very Large Scale Integration (VLSI) design. The program aimed to provide valuable insights into the diverse job roles available in the VLSI industry

"Career Opportunities through GATE Examination"

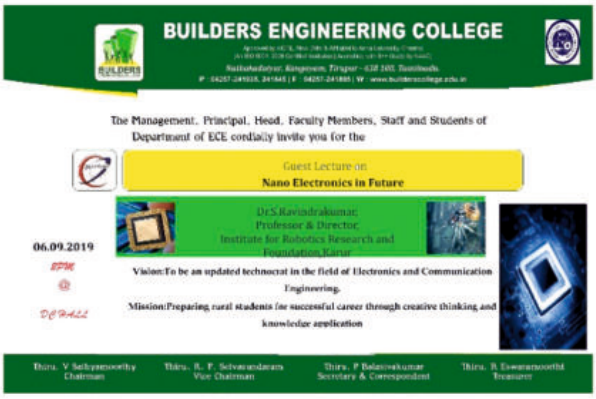
September 23, 2019



.On September 23, 2019, a seminar titled "Career Opportunities through GATE Examination" was organized by the student association "GNAANA" and the Indian Society for Technical Education (ISTE) at Builders Engineering College, Kangayam. The seminar aimed to provide insights into career paths and opportunities available through the Graduate Aptitude Test in Engineering (GATE) examination. The session was conducted by Mr. V. Kumar, and Mr. M. Shanmugham. Both educators shared valuable information and guidance regarding the GATE examination, shedding light on various career possibilities for engineering students. The collaborative effort between the student association, ISTE, and the active participation of speakers demonstrated their commitment to guiding and mentoring students towards successful career endeavours.

"Nano Electronics in Future"

September 6, 2019

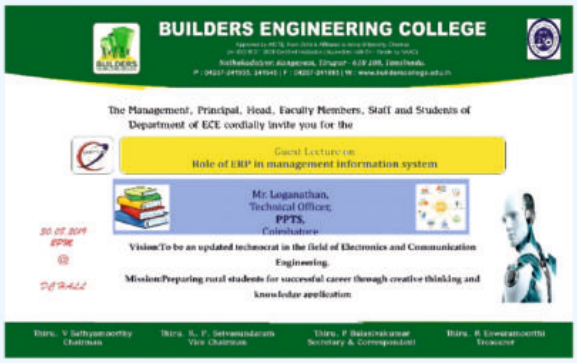


On September 6, 2019, a seminar titled "Nano Electronics in Future" was organized by the student association "GNAANA" and the Indian Society for Technical Education (ISTE) at Builders Engineering College, Kangayam. The session featured Dr. S. Ravindrakumar, Professor and Director of the Institute for Robotics Research and Foundation in Karur, as the guest speaker. The seminar provided valuable knowledge and perspectives on the advancements and potential applications of nanotechnology in electronics. This event, which aligns with Program Outcomes of engineering education showcased the commitment of the student association, ISTE, in promoting awareness and understanding of emerging technologies among the students at Builders Engineering College

"Role of ERP in Management Information System"

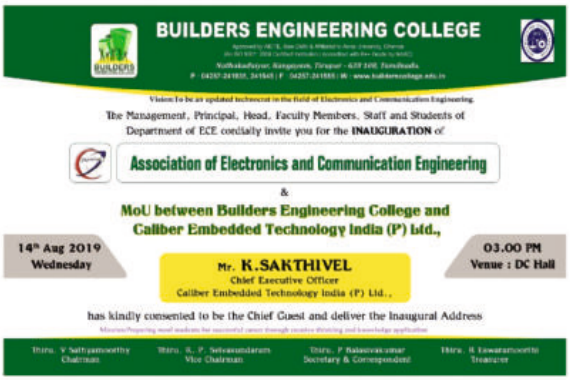
August 30, 2019

The Guest Lecture on the Role of ERP in Management Information Systems successfully integrated key Program Outcomes, providing students with valuable insights into modern tool usage, fostering communication skills, and instilling the importance of lifelong learning in the rapidly evolving landscape of information systems management.



Association Inaugural & MoU with Caliber Embedded Technology India (P) Ltd.

August 14, 2019



On August 14, 2019, a significant event took place, namely the "Association Inaugural & MoU with Caliber Embedded Technology India (P) Ltd., Coimbatore." This event was organized by the student association "GNAANA" and the Indian Society for Technical Education (ISTE). The inauguration and Memorandum of Understanding (MoU) signing ceremony marked the collaboration between the student association and Caliber Embedded Technology India (P) Ltd., Coimbatore. Mr. K. Sakthivel, CEO of Caliber Embedded Technology India (P) Ltd., Coimbatore, graced the occasion.

MOU SIGNED

Caliber Embedded Technology India (P) Ltd., Coimbatore

The Memorandum of Understanding (MoU) signing ceremony symbolized a pivotal collaboration between the student association and Caliber Embedded Technology India (P) Ltd., headquartered in Coimbatore. Spearheading the event was Mr. K. Sakthivel, esteemed CEO of Caliber Embedded Technology India (P) Ltd., Coimbatore. The ceremony not only underscored a formal agreement but also heralded a promising partnership set to foster mutual growth and innovation. With this collaboration, both entities aim to leverage their respective strengths and expertise, amalgamating academia with industry seamlessly. Through shared resources, knowledge exchange, and collaborative projects, the partnership seeks to enhance educational opportunities for students while addressing industry needs effectively. The MoU signing ceremony serves as a cornerstone, embodying the spirit of cooperation and advancement towards common goals.

STUDENT ACHIEVEMENT

On December 18, 2019, Mr. S.P. Devaraja participated in the 19th ISTE TN Section Annual Convention of Engineering Students held at PSG Institute of Technology and Applied Research. During the convention, he was honoured with the ISTE Chapter Best Student Award. This recognition typically acknowledges outstanding contributions, leadership, and excellence in academic and extracurricular activities. Such awards play a significant role in motivating students and encouraging a culture of achievement within the academic community.

Mr. S.P. Devaraja's receipt of the ISTE Chapter Best Student Award highlights his dedication and notable contributions to the engineering community during the convention.

IN PLANT TRAINING

All India Radio, Coimbatore

During the academic year 2019-2020, twelve Electronics and Communication Engineering (ECE) students underwent a rewarding Inplant Training at All India Radio, Coimbatore, spanning from June 10 to June 14, 2019. This initiative aimed to furnish students with practical exposure to the broadcasting industry, bridging the gap between theoretical knowledge and real-world applications. The diverse list of participants included Abitha G, Bharathi V, Dhivya Sri S, Gnanaprakash R, Haripriya A, Jayavignesh R L, Kowsalya M, Muthu Vignesh B, Nagarajan C, Nandhini R, Pavithra V, and Sridhar A. The training, hosted at the esteemed venue of All India Radio, Coimbatore, centered around objectives such as gaining hands-on experience in radio broadcasting technologies, understanding the functioning of transmission and reception systems, and acquiring insights into the production and editing processes of radio content. Activities included technical exposure sessions covering equipment handling and maintenance, as well as opportunities for participants to observe and engage in the production, scripting, and editing of radio content. Positive feedback from participants highlighted the appreciation for practical knowledge gained, an enhanced understanding of broadcasting technologies, & exposure to the real-world work environment within the broadcasting industry.

Caliber Embedded Technology India (P) Ltd., Coimbatore

In the academic year 2019-2020, students underwent an extensive Inplant Training program at Caliber Embedded Technologies in Salem, spanning from December 3 to December 7, 2019. The primary objective of this training initiative was to equip students with practical experience in embedded technologies, thereby enhancing their skill set and providing exposure to the industry landscape.

The training program focused on several key objectives, including gaining practical exposure to embedded systems and technologies, understanding the intricacies of design and development processes, acquiring hands-on experience with industry-standard tools and platforms, and exploring real-world applications of embedded technologies.

Participants immersed themselves in various activities, including intensive sessions on embedded system design, practical hands-on exercises with embedded tools and programming languages, and engaging in project-based learning to solve real-world problems. Moreover, interaction with professionals at Caliber Embedded Technologies offered invaluable insights into industry practices and expectations.

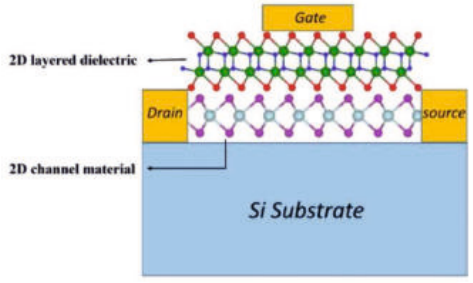
Feedback from participants highlighted their satisfaction with the practical exposure gained, improved understanding of embedded systems design and development, enhanced proficiency in using industry-standard tools and platforms, and valuable exposure to the work culture and expectations of the embedded systems industry.

STUDENT CORNER

Ultrathin Dielectrics for 2D Devices

by ***Ms. A. Ayisha Banu, II ECE***

Ultrathin dielectrics play a crucial role in the development of 2D devices, particularly in the field of nanoelectronics. 2D materials, such as graphene and transition metal dichalcogenides (TMDs) like molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), have unique electronic properties that make them promising candidates for next-generation electronic devices.



Dielectrics are insulating materials that are essential for building transistors and other electronic components. In the context of 2D devices, ultrathin dielectrics serve several purposes:

Gate Insulator in Transistors:

In field-effect transistors (FETs), the dielectric layer serves as the gate insulator. The thickness of this dielectric layer is critical for controlling the flow of electrons between the source and drain terminals. Ultrathin dielectrics are desirable because they enable better electrostatic control, minimizing leakage currents and improving device performance.

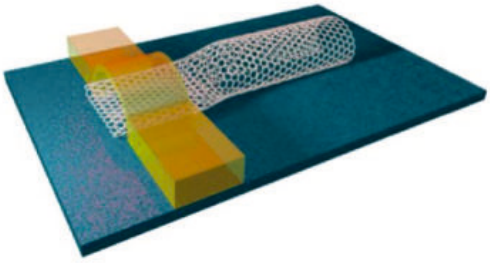
Capacitors and Energy Storage:

Ultrathin dielectrics are also used in capacitors for energy storage applications. The thinness of the dielectric layer enhances the capacitance, which is crucial for applications like energy storage devices and capacitive sensors.

Carbon Nanotube Digital Electronics

by *Mr. Jaya Vignesh, III ECE*

Carbon nanotubes (CNTs) have garnered significant interest in the field of digital electronics due to their unique electronic properties. CNTs are cylindrical structures made of carbon atoms arranged in a hexagonal lattice, and they can exhibit both metallic and semiconducting behavior depending on their chirality. These properties make them attractive for various electronic applications, including digital circuits. Here are some key aspects of carbon nanotube digital electronics



Transistors:

Carbon nanotube field-effect transistors (CNTFETs) are a key component in carbon nanotube digital electronics. CNTFETs can be either semiconducting or metallic, and researchers have focused on utilizing semiconducting CNTs to build transistors for digital circuits.

High Carrier Mobility:

One of the significant advantages of CNTs is their high carrier mobility. Electrons can move rapidly through carbon nanotubes, enabling the development of high-speed transistors. This property is crucial for achieving high-performance digital circuits.

Reduced Power Consumption:

CNTFETs have the potential to operate at lower power consumption compared to traditional silicon-based transistors. This is attributed to the excellent electrostatic control and low off-state leakage current in CNTFETs.

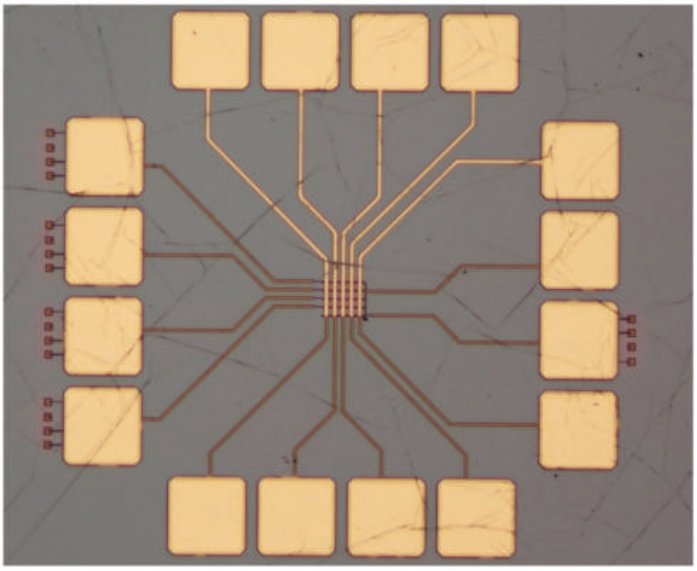
Scalability:

Carbon nanotubes are nanoscale materials, and their dimensions make them suitable for scaling down electronic devices to the nanoscale. This scalability is advantageous for achieving higher integration densities and packing more transistors on a chip.

A Hybrid Memristor–CMOS Chip for AI

by *Ms. M. Juvairiya, II ECE*

A hybrid memristor–CMOS (Complementary Metal-Oxide-Semiconductor) chip refers to a combination of memristive devices and traditional CMOS technology on a single integrated circuit. This hybrid approach leverages the advantages of both memristors and CMOS to create a more efficient and capable platform, particularly for artificial intelligence (AI) applications. Here are some key points about a hybrid memristor–CMOS chip for AI



Memristors:

Memristors are a type of non-volatile memory device that can store and process information. They have the unique property of changing their resistance based on the history of applied voltage. This property makes them suitable for use in neuromorphic computing, where emulating the synaptic behavior of the human brain is a key goal.

Advantages of Memristors:

Memristors offer several advantages, including non-volatility, low power consumption, and the ability to perform both memory and processing functions in the same device. These characteristics make memristors well-suited for neuromorphic computing, which is an approach to AI that mimics the structure and function of the human brain.

CMOS Technology:

CMOS technology is the mainstream technology used in the fabrication of integrated circuits. It is well-established, cost-effective, and widely used in the

semiconductor industry. CMOS circuits are known for their reliability and efficiency in digital logic operations.

Integration of Memristors and CMOS:

The integration of memristors with CMOS technology allows for the creation of hybrid chips that can take advantage of the strengths of both technologies. Memristors can be used for synaptic functions in neuromorphic circuits, while CMOS components handle traditional digital logic and control functions.

Neuromorphic Computing:

Neuromorphic computing aims to build computational systems that mimic the structure and function of the human brain. Memristor–CMOS hybrid chips are particularly relevant in this context because memristors can emulate the synaptic plasticity essential for learning and memory, while CMOS provides the necessary digital processing capabilities.

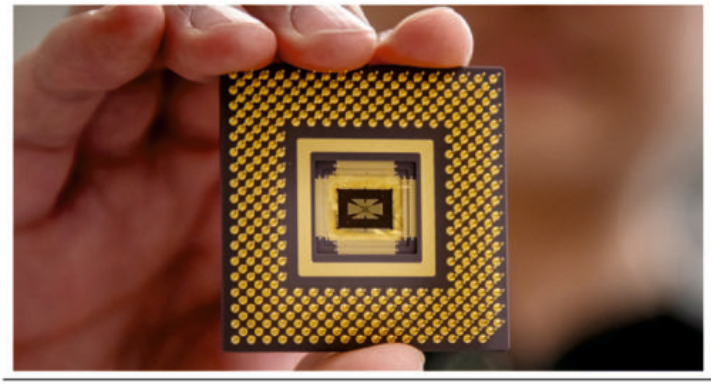
Energy Efficiency and Parallel Processing:

Memristors, with their ability to perform analog operations and store information, contribute to energy-efficient computing. The parallel processing capabilities of memristors align well with the parallel nature of neural networks, making them suitable for accelerating AI tasks.

Research and Development:

The development of hybrid memristor–CMOS chips is an active area of research. Researchers are exploring various architectures and fabrication techniques to optimize the integration of memristors with CMOS technology, addressing challenges related to compatibility, scalability, and reliability.

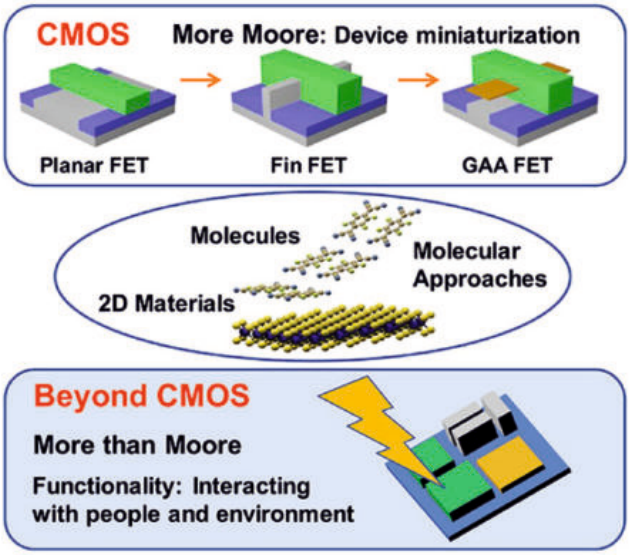
By combining memristors and CMOS on a single chip, researchers aim to create more efficient and powerful computing platforms for AI applications, particularly in the emerging field of neuromorphic computing. These hybrid architectures have the potential to revolutionize the way AI tasks are performed, offering improvements in speed, energy efficiency, and adaptability.



Beyond CMOS Technologies: Pioneering the Future of VLSI Circuits with Novel Materials and Emerging Technologies

by *Mr. Jaya Vignesh, III ECE*

The relentless demand for smaller, faster, and more energy-efficient electronic devices has fueled a quest for alternatives to traditional Complementary Metal-Oxide-Semiconductor (CMOS) technology in Very Large Scale Integration (VLSI) circuits. This article delves into the exciting realm of Beyond CMOS technologies, exploring novel materials and emerging technologies that hold the promise of revolutionizing the landscape of future VLSI circuits.



The Limitations of CMOS Technology

While CMOS technology has been the workhorse of the semiconductor industry for decades, it faces inherent limitations as device dimensions shrink and power densities rise. Issues such as leakage currents, power consumption, and the physical constraints of traditional silicon-based devices necessitate the exploration of alternative technologies to sustain the trajectory of Moore's Law.

Spintronics: Harnessing Electron Spin for Information Processing

Spintronics, short for spin transport electronics, represents a paradigm shift from traditional charge-based electronics to utilizing the intrinsic spin of electrons for information processing. In spintronic

devices, the spin state of electrons, rather than their charge, is manipulated to store and process information. This technology holds the potential for non-volatile, low-power memory and logic devices.

Applications:

Spin-Transfer Torque MRAM (STT-MRAM): Non-volatile magnetic random-access memory with fast read and write times.

Spin-FETs: Spin-based field-effect transistors that leverage electron spin for logic operations.

Advantages:

Reduced power consumption due to lower switching energy requirements.

Non-volatility for data retention without constant power supply.

Tunnel Field-Effect Transistors (TFETs): Overcoming the Subthreshold Swing Limit

TFETs represent a departure from conventional MOSFETs by exploiting quantum tunneling for carrier injection. This technology addresses the fundamental limitation of subthreshold swing in MOSFETs, offering the potential for steep subthreshold slopes and reduced off-state leakage.

Applications:

Low-power digital and analog circuits where subthreshold swing is critical.

Energy-efficient logic gates in VLSI circuits.

Advantages:

Improved subthreshold slope leading to lower power consumption.

Enhanced performance at lower supply voltages.

2D Materials: Unleashing the Potential of Atomically Thin Layers

The family of 2D materials, including graphene and transition metal dichalcogenides (TMDs), exhibits extraordinary electronic properties due to their atomically thin structure. These materials offer unique possibilities for nanoscale devices and are explored for various VLSI applications.

Applications:

Graphene FETs: Leveraging the high electron mobility of graphene for high-speed transistors.

TMD-based transistors: Utilizing the semiconducting properties of TMDs for electronic devices.

Advantages:

Atomically thin layers enable excellent electrostatic control.

Potential for flexible electronics and unconventional device geometries.

Challenges and Future Directions

While Beyond CMOS technologies show immense promise, several challenges must be addressed for their successful integration into VLSI circuits:

Fabrication Techniques:

Developing scalable and cost-effective fabrication techniques for Beyond CMOS devices is crucial for their widespread adoption.

Materials Integration:

Efficiently integrating novel materials into existing silicon-based processes and designing hybrid circuits that leverage the strengths of different materials.

Reliability and Stability:

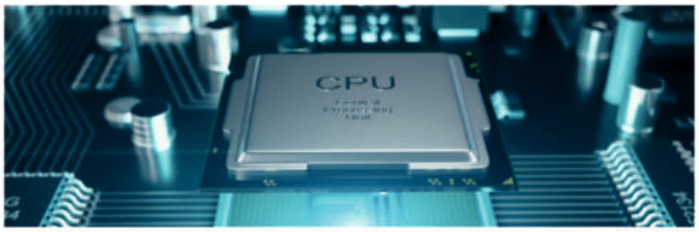
Ensuring the long-term reliability and stability of devices based on new materials, especially in the context of fluctuating environmental conditions.

Manufacturing Consistency:

Achieving consistent manufacturing yields and minimizing variations in device performance across a large-scale production.

Conclusion:

Beyond CMOS technologies stand at the forefront of the next wave of innovation in VLSI design, offering solutions to the challenges posed by the limitations of traditional CMOS. Spintronics, TFETs, and 2D materials showcase the diversity of approaches in harnessing novel physical phenomena for information processing. As researchers and engineers continue to explore these technologies, overcoming challenges and refining fabrication processes, the transition from CMOS to Beyond CMOS promises to unlock new dimensions of performance, energy efficiency, and versatility in the world of VLSI circuits. The journey beyond CMOS is not just a technological evolution but a leap into a future where the boundaries of electronic possibilities are redefined.



Foldable & Flexible Displays

by ***Mr. S.P. Deva Raja, IV ECE***

In the ever-evolving landscape of electronic devices, one of the most intriguing and transformative trends that emerged in recent years is the development of foldable and flexible displays. These cutting-edge technologies have the potential to reshape the way we interact with our devices, offering new possibilities in terms of design, functionality, and user experience. In this article, we will delve into the advancements in foldable and flexible display technology, exploring the key players, the challenges faced, and the potential implications for the future of consumer electronics.

The Evolution of Displays

The journey towards foldable and flexible displays began with the relentless pursuit of innovation in the realm of traditional rigid displays. Over the years, we have witnessed the evolution from bulky cathode-ray tube (CRT) displays to sleek and energy-efficient liquid crystal displays (LCDs) and organic light-emitting diode displays (OLEDs). However, as consumer demand for more portable and versatile devices increased, the limitations of rigid displays became apparent.

Challenges and Breakthroughs

The journey to perfecting foldable and flexible displays has not been without its challenges. One of the primary hurdles has been developing materials that can withstand constant folding without compromising durability or display quality. The use of flexible materials such as plastic OLED (POLED) has become common, but researchers continue to explore advanced materials to enhance longevity.

Durability concerns also extend to the display itself. The delicate nature of foldable displays requires precision engineering to prevent damage from repeated folding and unfolding. Manufacturers have invested in robust hinge mechanisms and protective layers to address these concerns and provide a reliable user experience.

Moreover, the user interface and user experience (UI/UX) design present unique challenges for developers working on applications optimized for foldable displays. Creating seamless transitions between different screen sizes, orientations, and modes is crucial for delivering a cohesive and intuitive user experience.

Despite these challenges, there have been notable breakthroughs. Advances in manufacturing processes and materials have contributed to more robust and reliable foldable displays. Improved hinge designs, like the ones seen in the Samsung Galaxy Z Fold 3 and the Huawei Mate X2, showcase the industry's progress in addressing durability concerns.

Applications Beyond Smartphones:

While foldable displays gained prominence in the smartphone market, their applications extend beyond handheld devices. Manufacturers are exploring the integration of foldable displays in laptops, tablets, and even wearable devices. The flexibility of these displays opens up possibilities for innovative form factors and multi-functional devices.

In the laptop arena, companies like Lenovo and Dell have introduced foldable laptops with screens that can be folded for portability or unfolded for a larger working area. This adaptability caters to users who value both the convenience of a compact device and the productivity of a larger display.

In the realm of wearables, companies are experimenting with smartwatches featuring foldable displays that can provide more screen real estate when needed. This could revolutionize the way we interact with information on our wrists, offering a more immersive experience without sacrificing portability.

The Future of Foldable Displays:

As the technology matures, the future of foldable displays holds exciting possibilities. The continued collaboration between material scientists, engineers, and electronics manufacturers will likely result in even more durable and versatile displays.

Conclusion:

The advent of foldable and flexible display technology represents a significant leap forward in the evolution of electronic devices. From smartphones to laptops and wearables, these displays offer a glimpse into a future where versatility and innovation converge.